ABSTRACT OF THE DISCLOSURE

Disclosed is a method for manufacturing multi-level interconnections using a dual damascene process. The method includes: forming a first interconnection line on a semiconductor substrate; forming a first interlayer insulating layer on the first interconnection line; forming a first etching stop layer on the first interlayer insulating layer; forming a via hole exposing the first interconnection line by selectively etching the first etching stop layer and the first interlayer insulating layer; forming etching stop patterns around an inlet of the via hole by selectively etching the first etching stop layer; forming a second interlayer insulating layer on the etching stop pattern and the first interlayer insulating layer; forming a trench by selectively etching the second interlayer insulating layer; and forming a conductive layer in the trench and in the via hole.